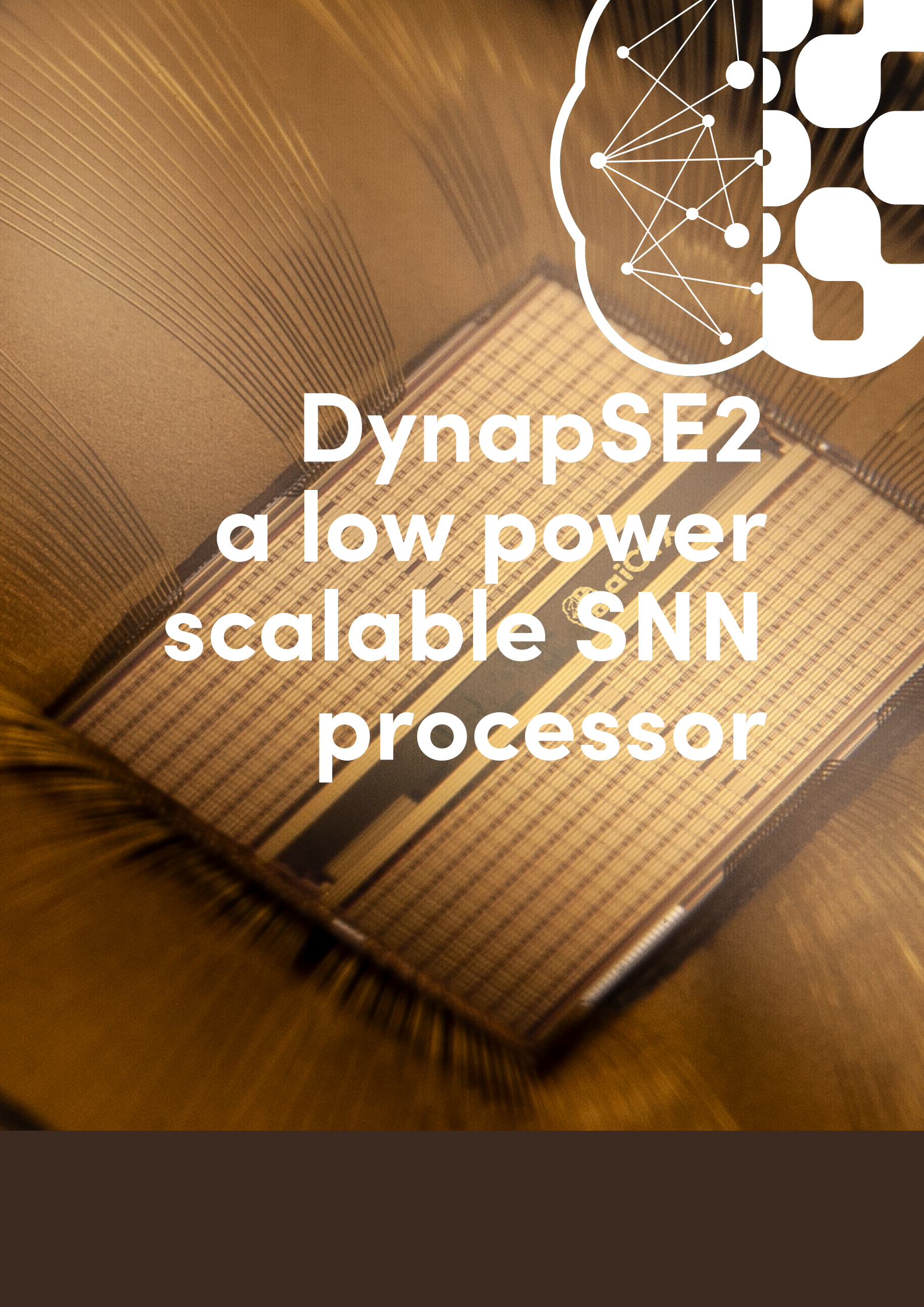

DynapSE2 a low power scalable SNN processor



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Our new neuromorphic chip combines the impeccable energy efficiency of its previous generations with **new features for low latency, real-time applications** *for general purpose recurrent and reservoir networks.*

With **integrated biosignal amplifiers and a direct dynamic vision sensor bus**, *the DynapSE2 is a perfect fit for* **mobile health and robotics applications**. *Each chip features 1k redesigned adaptive exponential integrate-and-fire analog ultra low-power spiking neurons and 65k enhanced synapses with configurable delay, weight and short term plasticity.*

The innovative asynchronous low latency communication infrastructure (patented) enables each neuron to communicate with up to 262k surrounding neurons. **Unlimited scalability via relay neurons permits emulation of truly large scale networks.**



Support for a wide range of network architectures

The DynapSE2

The DynapSE2 is a mixed signal Spiking Neuronal Network (SNN) Processor. Based on design principles taken from biological nervous systems, it uses analog signal processing and digital event based communication, just like our brain.

Combining this with weak inversion aVLSI design methods — also known as sub-threshold design — provides the DynapSE2 with impeccable energy efficiency. Our clock free design runs in native real time and the asynchronous communication scheme ensures very low latencies.

Each DynapSE2 chip has 1024 neurons distributed over 4 individually configurable Neural Cores, connected by a patented hierarchical routing grid. The tag-based routing infrastructure provides direct communication from one chip to 16 × 16 surrounding chips, connecting up to 262k neurons.

Supported models and network architectures

The tag based routing system used by DynapSE2 permits a wide range of network models to be implemented. The neuron model itself is highly modular, and all optional features can be fully bypassed. The result is a neuromorphic emulation platform that can implement a wide range of neuronal and network dynamics.

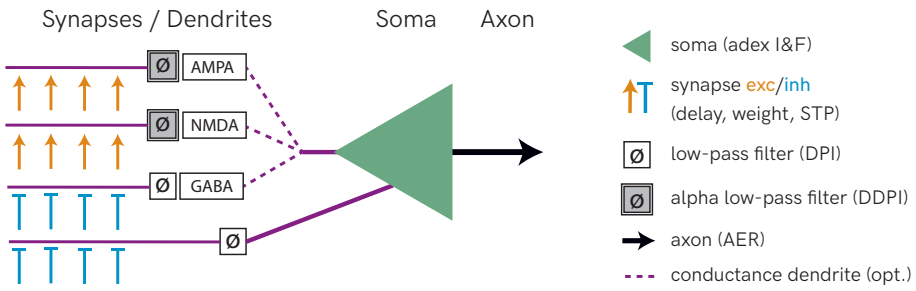
Neuron model

The heart of the DynapSE2 is the exponential integrate and fire somatic model. Each physical neuron runs in real time and emulates complex neuron behaviour.

Each neuron is composed of Somatic, Dendritic and Synaptic blocks.

The Synaptic block comprises 64 content addressable memory (CAM)-based synapses per neuron, with 4 bit weights. Each synapse can be attached to any of the 4 dendritic compartments.

The Dendritic block contains 2 excitatory and 2 inhibitory differential pair integrator-based low-pass filter compartments, which elicit excitatory and inhibitory post synaptic potentials (EPSP / IPSP). PSPs can accurately emulate alpha function synapse potentials.



A sophisticated neuron model permits a wide variety of synaptic, dendritic and somatic dynamics to be emulated. The DynapSE2 neuron supports advanced biophysically-realistic neuronal behaviours.

The Somatic block models an exponential or linear Integrate and Fire (IAF) neuron, with optional firing-rate adaptation.

The textbfAMPA dendritic compartment offers an optional 1D or 2D resistive grid, to diffuse incoming EPSPs between nearby somas.

The NMDA dendritic compartment can gate the incoming current depending on the somatic membrane potential.

Both the AMPA and NDMA excitatory dendritic compartments, as well as the GABA inhibitory compartment, can be individually switched to conductance mode, to emulate a large class of biologically inspired synaptic models.

Feed forward networks

Feed forward networks are the simplest possible network architecture. They process events as they move through the layers of the network.

Sparse feed forward networks are built by dividing available neurons into layers, and forming unidirectional synaptic connections between layers.

Dense feed forward networks can utilize advanced tag compression, with an additional option in each core to reduce the number of neurons by 4 to have 256 CAM synapses per neuron.

Time-to-first-spike and timed networks

Time-to-first-spike computation relies on latency of spike waves travelling through a network.

To support delay based networks, each synapse can be configured to one of 4 delay classes. Two synaptic delay classes are precise; and the other two classes provide a controlled distribution of delays. This enables precise time-to-first-spike, and randomly timed networks. Delays of up to 500 ms are supported[1].

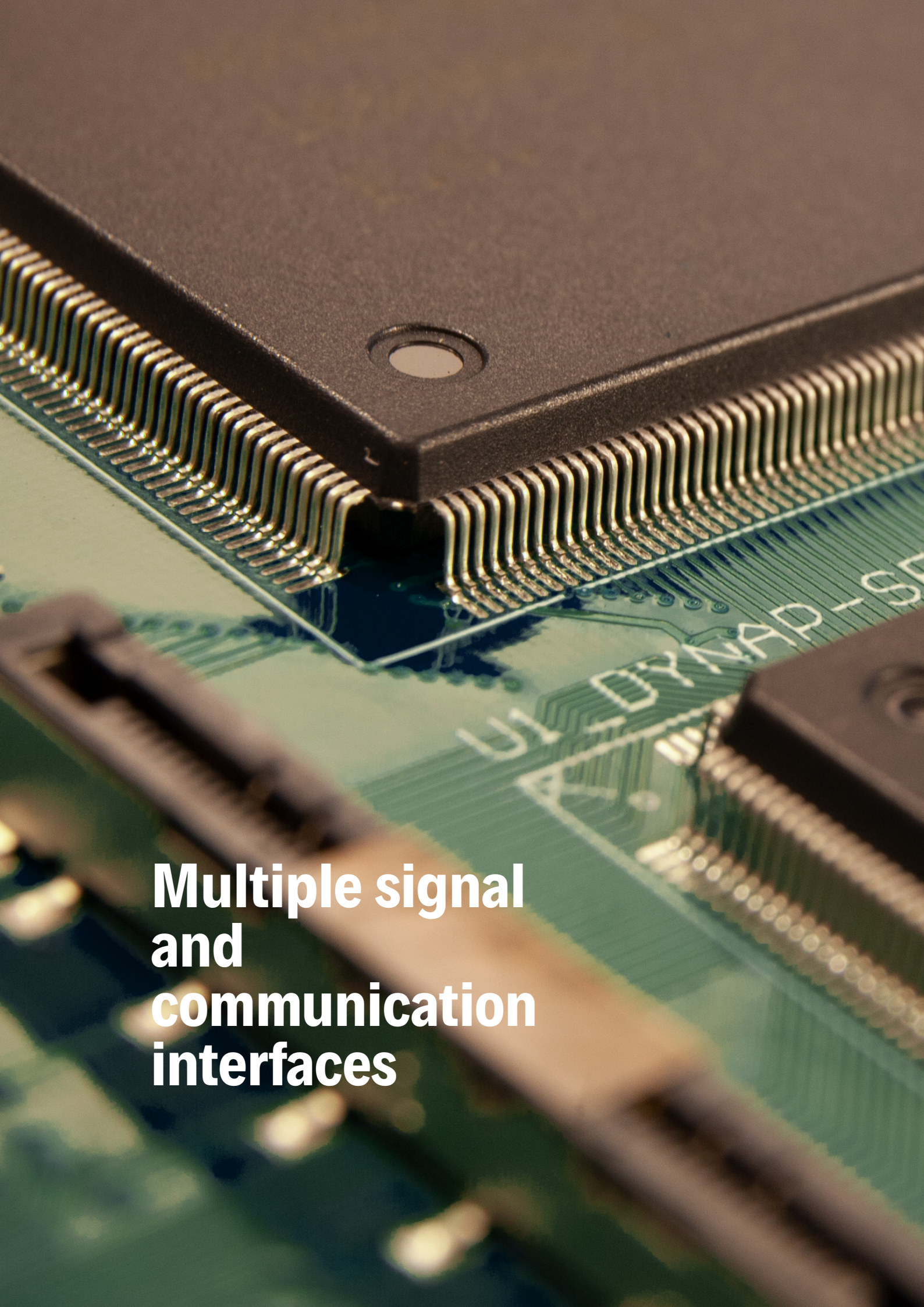
Recurrent and reservoir networks

Reservoir networks use recurrent connections between neurons to build complex network dynamics supporting a "memory trace" of their activity over time.

The fully parallel nature of the hardware makes the DynapSE2 the perfect fit for recurrent networks. To keep the reservoir stable over long periods of time we include optional homeostatic mechanisms, which adapt the firing activity of neurons in the network. The homeostasis time constants can be set to up to 1 day[1].

[1] Values based on SPICE simulations. Values may differs in the final product.

Additionally, optional **synaptic short term depression** can be used to enhance the memory lifetime in special-designed reservoir networks.



Multiple signal and communication interfaces

Supported Interfaces

The DynapSE2 provides a variety of interfaces for analog input signals, event-based communication, configuration and monitoring.

Inter chip communication

Each chip has asyncronus 4 high speed address event representation (AER) buses to enable network scalability (DynapSE2) across a two dimensional grid, each chip can directly address a neighborhood of 16x16 chips.

On chip monitoring

64 on-chip, current-based spiking analog to digital converters (sADC) ensure easy monitoring of all relevant neural signals. This enhances the configuration experience and usability hugely.

Dynamic vision sensor input

The DynapSE2 supports direct AER input from the dynamic vision sensors (DVS) from iniVation AG (DAVIS346, DAVIS240, DVS128) as well as Prophesee's ATIS cameras. It supports hot pixel filtering, region

of interest selection, cropping and subsampling, as well as passing the AER input on to the next chip for multi region processing.

Biosignal interface

DynapSE2 includes an 8-channel biosignal amplifier and delta sADC for brain machine interface applications and biosignal monitoring. The amplifier operates in the 1-40dB[2] range and multiple bandpass channels can filter incoming signals in parallel. The 64 sADC channels encode the signals using a delta spike encoding which can be directly processed by the Neural Core of DynapSE2.

[2] Values based on SPICE simulations. Values may differs in the final product.

About aiCTX

aiCTX is a commercial spin-off from the Institute of Neuroinformatics, University of Zurich and ETH Zurich. We specialize in developing mixed-signal neuromorphic silicon hardware for neural simulation and signal processing; develop software for interfacing with and configuring neuromorphic hardware; and develop solutions to analyse and process bio-signals.

“ aiCTX specializes in developing low-power neuromorphic silicon hardware ”

aiCTX is developing approaches for bio- and industrial-signal processing, based on biologically-inspired neuronal architectures emulated on low-power neuromorphic hardware. The neuromorphic industry is growing rapidly, with significant contributions from large players such as Intel and IBM. Our advantages are our long experience in designing low-power neuromorphic circuits, and our experience in theory of neuromorphic and cortical computation.

aiCTX is also developing solutions for rapid event-driven processing of visual information, for application in industrial monitoring and automotive markets. We are building the first commercially available full-stack neuromorphic hardware solutions.

Key personnel

Dr. Ning Qiao, PhD — *CEO, CTO, co-founder*
Dr. Qiao is an expert analog and mixed-signal neuromorphic engineer, and holds the position of Chief Executive Officer at aiCTX. Dr Qiao designs next-generation mixed-signal neuromorphic circuits for rapid event-driven processing. He is the founder, CEO and CTO of aiCTX.



Prof. Dr. Giacomo Indiveri, PhD — *CSO, co-founder*
Prof. Dr. Indiveri is an expert neuromorphic engineer, with more than 20 years' experience in analog and mixed-signal hardware design, and extensive experience managing the development of neuromorphic computing hardware. He holds the positions of Chief Science Officer at aiCTX, as well as Director of the Institute of Neuroinformatics at the University of Zurich and ETH Zurich.



Dr. Kynan Eng — *Chairman, co-founder*
Dr. Eng is a co-founder and chairman of aiCTX. He has led startups to successfully closed funding rounds and product launches (YouRehab, iniVation), and has worked at companies including ABB, Alstom and a network management supplier for Telstra. He holds degrees in computer science and mechanical engineering from Monash University, and a PhD from the ETH Zurich, where he also led a research group investigating the neuroscience of virtual reality interactions.



Francois Stieger — *Board advisor*
Mr Stieger is an experienced executive, investor and board advisor. He has served in senior management roles at Verisign, Oracle, and Broadvision, where he was involved in the IPO and listing on NASDAQ. He is a former partner at Amadeus Capital and is currently active in S-Partners and in other investment vehicles.



Ole Richter — *R&D Engineer, Analog and Mixed Signal IC engineer*
Mr Richter is a specialist in analog and mixed-signal neuromorphic IC design, with substantial experience in applications and design of neuromorphic hardware. Mr Richter holds a Masters of Sciences degree in Neural Systems and Computation from the University of Zurich and ETH Zurich, and a Bachelor of Science in Cognitive Informatics from Bielefeld University.

Forward-looking statements disclaimer

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3. execution of the Company's vision and growth strategy;
4. sources and availability of third-party financing for the Company's projects;
5. completion of the Company's projects that are currently underway, in development or otherwise under consideration;
6. renewal of the Company's current customer, supplier and other material agreements; and
7. future liquidity, working capital, and capital requirements.

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